4. Theory of Operation

4.1 Processor Board : F9601-11-16, F9601-11-64, F9602-1-64

MPC603e Processor

This processor board is based on the Power MPC603e processor.
It is a 64-bit RISC processor with 2x32kbyte cache. It features high speed processing and fast memory accesses.
The F9601-11-x processor is set to an internal clock of 96MHz and the F9602-1-64 is set to an internal clock speed of 200 MHz. They are both used in a 32-bit mode.

There are two “worlds” on the board:

- the 32-bit world, including the main PowerPC processor, the dynamic RAM modules and the VGA interface;
- the 8 or 16-bit world, including all other on-board peripherals, external small peripherals and acquisition board.

A MC68150 dynamic bus sizer is used as an interface between the two worlds.

Power Supplies

The board uses three power supplies from the main acquisition board: Vcc, +15V and -15V. Vee is wired on a connector for board test purposes.
The +15V supply OP-amps on the 9601-11 board, and +15V and -15V supply small peripherals.
The current processor needs a 3.3V power supply, all the rest of the logic needs 5V. All signals are TTL compatible.
The PLL circuit (88916) generates a PLL_LOCK signal, which is used to clamp the 3.3V and 2.5V references as long as the 32MHz clock is not stable. The processor also needs to be protected against too big voltage differences between 2.5V and 3.3V (diodes on the reference).
An OP-amp and a MOSFET transistor for each power supply are used. The reference voltages are taken directly from the 5V power supply by a resistive divider.
Capacitors and a few diodes ensure that the supplies do not exceed dangerous levels at power-up, nor rise too fast.

32-bit Peripherals

There are only three devices hooked up on to the processors 32-bit data bus:

- the VGA video controller
- the DRAM system
- the bus sizer, bridge to the 68k-like world

Processor Block Diagram

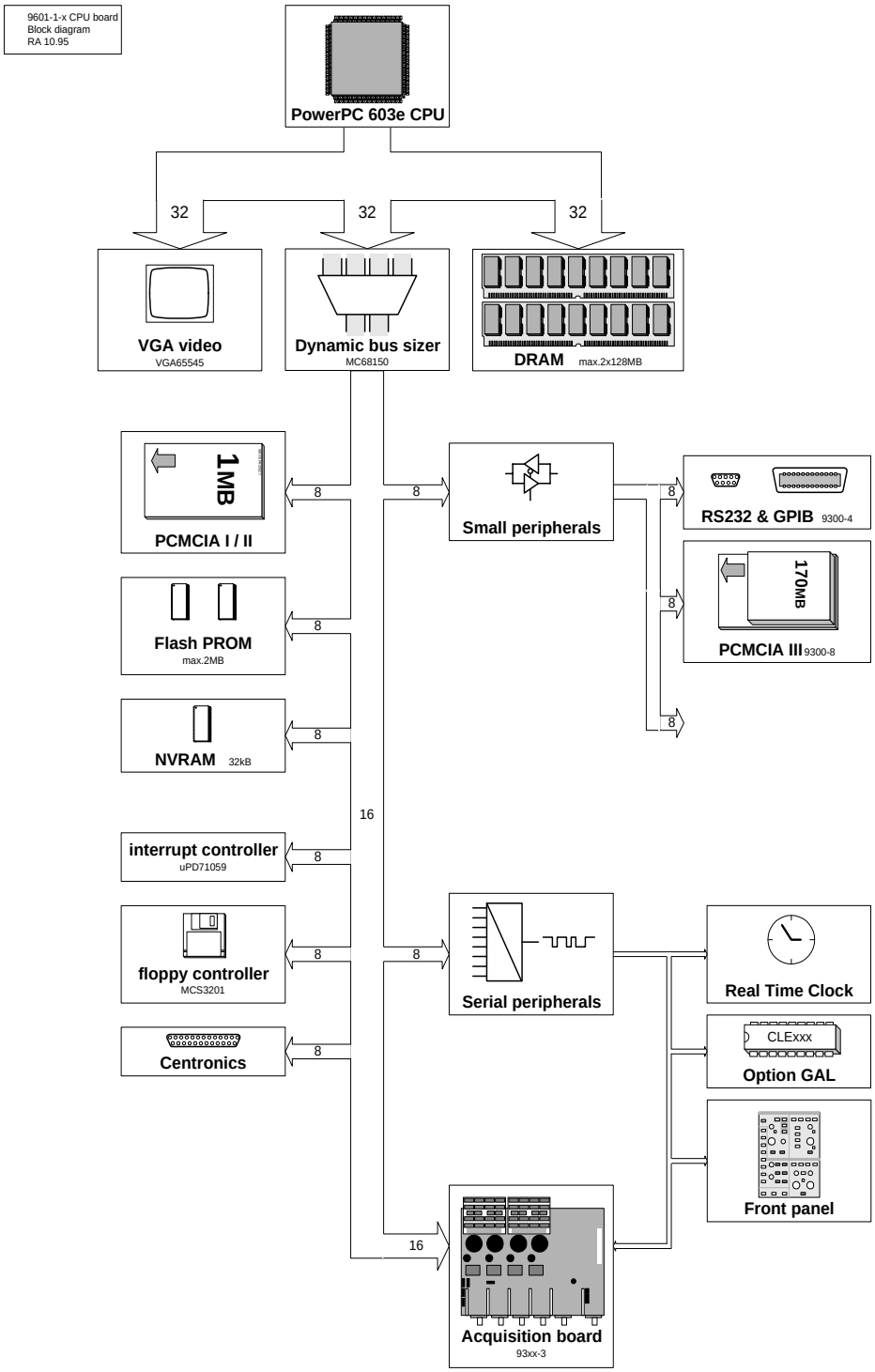

Fig 4-1: 9601-11 Block diagram

DRAM

The DRAM consists of two SIMM modules from 4 MB up to 32 MB each.
By interleaving two SIMMs, the access time is dramatically reduced (one beat every 30ns, while the other module “recovers” from the previous access).
The DRAM control logic, including refresh control, is built around several GALs and a few gates.
RAMEUR (A44) is the main sequencer. It inserts refresh cycles whenever needed, and drives row and column addressing timing.
RASADE (A39) controls the row address select lines of the memory modules, and generates the addresses for double beat or burst accesses.
OCCASE (A37) generates the column address select lines of the SIMMs.
DRAME (A57) holds some glue logic, and a state machine that counts the number of beats, inserting pauses in the access if necessary (single SIMM support).
Four multiplexers (A40, 42, 46 and 47) switch between odd and even addresses to be sent to the address lines of the modules. One more multiplexer (A38) switches low order address bits, routing them either directly to the processor, or to the DRAM address generator in RASADE.

Normal Access Timing

This is the simplest access possible: the processor puts an address onto the address bus, and reads back or writes one long word (32-bit wide) to DRAM. Depending on the address (odd or even), bank A or bank B is selected in a dual SIMM configuration.

Burst Access Timing

A burst access on a 603e configured as a 32-bit device, consists of either two (“double beat”) or eight (“burst”) successive reads in DRAM. The idea is to put a start address onto the address bus, and read back or write several data’s from or to DRAM every clock cycle, without the processor incrementing the address (this is done by the external logic). To increase system performance, the memory has been interleaved, allowing each module to access a memory location every 60ns, but with a delay of 30ns between the modules.
A burst access is signaled by an active low _TBST signal and a 32-bit access (SIZ2..0= 011), a double-beat access is indicated by a high _TBST but an access size of 64 bits (SIZ2..0= 100). The double-beat case is decoded by a GAL (VIADUC), and the signal is named _DBEAT (active low).

Refresh Timing

The 32 kHz clock from the real time clock chip is used to refresh periodically the DRAM.
The GAL RAMEUR generates the refresh cycles, as well as the sequencing of _RAS and _CAS. Depending on the operating mode, it chooses to access slot A or selects alternately slots A and B.

Memory Mapping

By default, the board is set to the biggest memory size possible. The software checks out for “holes” in the addressing space, and sets accordingly two configuration lines, MAP1 and MAP0.

MAP1..0	meaning
00	2x4, single sided SIMMs
01	2x8 MB SIMMs
10	2x32 MB SIMMs

VGA

The VGA 65545 controller chip (A27) includes its own address decoding logic. It generates all video signals (red, green and blue video, horizontal and vertical syncs, and all control lines to drive a flat panel) and controls its associated 1 MB video dynamic RAM (reads, write and refresh cycles).
All timings are extracted from the 16 MHz bus clock, so no external crystal or timebase is needed.

The horizontal and vertical sync. signals are sent to both the internal and the external video connector (high density DB15 on the 9601-2 board). The external syncs are direct, the internal syncs pass through the GAL VIADUC (A32), allowing to force these two lines to ground. This puts the internal display in power down mode (standby mode).
The chip can support several bus interfaces (PCI, ISA, VL,), it is configured as VL-bus.

The 65545 chip generates red, green and blue video signals. These are controlled-impedance lines (37.5 Ohm approximately, which corresponds to two 75 Ohm loads in parallel). A low-pass filter is implemented right at the outputs from the VGA controller, and another low-pass filter is located at each video connector on the 9601-2 board (just after the “active” load).

9601-2 Board: VGA proper termination (auto termination)

The 9601-2 board is a complement to the 9601-11 main processor board. It holds the external Centronics connector (female DB-25) with its EMI filters, both internal and external VGA connectors (female mini DB-15), and line termination for R, G and B signals.

The VGA controller is able to drive a load of 37.5 Ohms on its Red, Green and Blue outputs (two 75 Ohms loads in parallel). The line impedance of these signals on the processor board is therefore close to 37.5 Ohms. The 9601-2 board includes a special termination circuit that keeps the loads on the R, G and B lines at 37.5 Ohms, no matter if one or two 75 Ohms loads are connected. The circuit assumes that a 75 Ohms load is present on each output.

Bus Sizer

The MPC603e processor does not support dynamic bus sizing, as did the 68k family. Many parts of the software and the hardware rely on that feature. A Motorola MC68150 chip ‘translates’ the PowerPC 32-bit data bus to a 68030 8 or 16-bit bus. Except DRAM and VGA controller, all peripherals work on this 68k-type bus. Full compatibility is therefore ensured with current acquisition boards and small peripherals.

16 and 8-bit Peripherals

The only 16-bit peripheral hooked on the bus is the acquisition board.
RETINE (A36) generates wait state timings and is used to switch between cold boot (return to default state) and warm boot (do a RESET, but keep current scope settings), and generates a bus error if max. access time is out and no peripheral has acknowledged the access.
ASSISE (A21) generates chip select signals for the bus sizer, BUDGET (A28) creates typical 68k signals (_BAS, _BDS, 16MHz clock).
The peripheral address decoding is done by a set of GALs (GRANDS (A20), PETITS (A29)) and a few multiplexers (A30, A22). GRANDS selects between main peripheral categories (VGA, DRAM, memory card, flash PROM, acquisition board or other peripherals), PETITS generates chip select signals for 8-bit peripherals (flash PROM, memory card, non-volatile RAM, Centronics and “others”). It also determines how many wait states are needed for peripherals not able to acknowledge a bus access. This is done by pulling low _DSACK0 after having sensed the corresponding number of wait states trough _BWT1 and _BWT3, which ends the current access.
The multiplexer A30 does a finer decoding between “others” decoded in PETITS, namely interrupt controller, small peripherals, serial interface, flash PROM chip 1 or 2, and status registers.

PCMCIA type I / II interface

This interface consists mainly of buffers for both data and address busses.
An OP amp (A10) and a MOS transistor (Q3) allow to switch off the memory card power supply while no card is plugged in, and turn it on slowly when plugged in.
The GAL CARDAN (A11) handles the card format and generates several control signals accordingly.
A16 (an hex D-type flip-flop) holds control bits for 12Vpp (flash programming voltage), DRAM memory mapping and memory card type. All bits of this register reset to zero when the _RESET signal goes active low, which means that their state is also guaranteed at power-up.
A9 and A12 are the read registers for several status bits.
Several EXOR gates (A17 and A18) invert the most significant address bits of the memory card whenever the SWAP jumper is plugged in, so that the first bytes are always located at 0xFFF00000, regardless of the size of the memory card. This allows to boot directly from a PCMCIA memory card.

Flash PROM

Two Intel 28F008-compatible 1MB PROMs (A24 and A25), are used.
From a hardware point of view, a flash PROM is the same as an EPROM in read mode. To write to it, however, a programming voltage (Vpp) needs to be applied to a pin. The 12V voltage is generated by a switching regulator (A26), controlled by a logic level (_EPPP).

NVRAM

This chip is powered through the lithium battery (VCT) when power is off. The chip select is held high through a pull-up resistor to VCT to avoid accidental overwriting while power is off.

Interrupt Controller

In order to keep compatibility with both 68k hardware and software, it is necessary to use a chip that prioritizes several interrupt sources. This is done by a NEC chip, an uPD71059. It scans eight interrupt pins and sends a unique interrupt to the processor when a (non-masked) interrupt appears.

Interrupt levels are assigned the following:

level 0	(lowest priority) acquisition board
level 1	small peripherals, unused
level 2	RS232
level 3	GPIB
level 4	small peripherals and acquisition board, unused
level 5	real time clock
level 6	time base (acquisition board)
level 7	(highest priority) only for test purposes. Linked to level 2 for debugging.

Floppy Controller

The floppy controller chip directly interfaces to a double or high-density disk drive. The floppy controller has a digital 8-bit input/output register, which is used to read several status lines from the drive (disk inserted, etc.).
In principle, the controller is able to provide an interrupt when accesses are completed. As these accesses are performed in non-time critical paths of the program, The interrupt line has been wired to the input register, so that the program has to poll this register until the interrupt line goes active.
The controller has it’s own timebase, a 24MHz crystal.

Centronics

Both external and internal Centronics ports are write-only. The data get latched in a 74HCT374 register (A45 for internal Centronics, A55 for external).

Small Peripheral Interface

This 8-bit interface is intended to allow external expansion to the processor board. A56 and A53 (74HCT541 tri-state buffers) buffer the address and control lines, and A62 (74HCT245, bi-directional tri-state buffers) buffer the data lines.
The address decoding is done on each peripheral board. The acknowledge for each access is also done by the peripheral device, so that there is no restriction on wait-states. The bus clock runs at 16mhz, and a reset line reinitializes the boards at the same time as the CPU.
Four interrupt lines are also included in this interface, so that interrupt-driven boards can be used (a good example is the 9300-4 GPIB/RS232 board, which uses interrupts 2 and 3).

Serial Interface for on-board Peripherals

Two GALs (SEVERE and SAVEUR) are used to access serial on-board devices, like the real time clock, option GAL, front panel and some parts of the acquisition board. The principle of such a serial access is the following:
every write or read to the serial interface allows to write or read one bit (the MSB of the byte). To write a byte to a serial device, you need eight accesses to the serial interface.
Many serial devices need the same protocol: you first send a command byte (read, write, clear, etc.), and then read or write one or several data (if required).
Depending on the address the serial interface is been accessed, the corresponding device gets selected (_SSER, _SFPR, _SLED or SRTC lines). A clock (_SCKA), a read data (SDRA or SDRD) and a write data (SDWA or SDWD) constitute the serial interface itself (the D suffix on read and write data lines means Digital, i.e. devices on the CPU board; an A suffix means devices on the Acquisition board).

RTC

The 68HC68T1 real time clock has several functions:

- keep a time-of-the-day and current-date information while the DSO is not powered on.
- generate a 32kHz clock for DRAM refreshment.
- generate a 128Hz periodic interrupt to force bus accesses from the processor (otherwise the watchdog timer would time out and reset the board) and allow periodic update of the time display (“scope alive”).

The chip uses it’s own 32.768kHz crystal to keep the time and derive all timings. A few discrete components around it leave the chip powered by the backup lithium battery while the rest of the board is not powered, and charge the battery when the power is on again.

Front Panel

The front panel LED can be controlled by a serial write access. The LED (write only) shares the same address as the option GAL (read only).
The LED is driven by the less significant bit (LSB) of the control register.

Watchdog and Reset Generation

The power supply is monitored by a TL7770-5 chip. Whenever the Vcc voltage goes below 4.8V (even for a short time !), a reset pulse is generated, whose width is determined by an RC time constant (33uF and internal resistor).
The second half of this chip serves as watchdog circuit. The processor needs to poll a sense line on that chip from time to time (typically a few ms). By doing this, a capacitor (33uF) is discharged. When not polled, it gets charged by a constant current, and when a given threshold is exceeded, a reset pulse is generated.
The LED connected goes off whenever the _RESET line is low, so a blinking LED indicates either no bus access for longer than a few hundreds of ms, or a problem (glitch) on the Vcc power supply.

Bus Error Generation

A bus error exception is generated when the _TEA pin is pulled low on the processor. The 603e expects a _TA signal as an acknowledge to the current data transaction, and inserts wait states as long as _TA has not been pulled low at the correct timing (refer to the MPC603e documentation for exact timing information's).
An external circuit is required to break the pending cycle if no device responds after a given time-out.
This is the job of the GAL RETINE (A36), which counts the number of wait states already passed (4 bit Gray counter). An external 4-bit counter (A59) extends the count to 160 (tbd) wait cycles before triggering a bus error.
An acknowledge (_DSACK1..0 lines) aborts the time-out count and finishes successfully the current cycle.

I/O Structure and GALs Involved

The following bloc diagram describes the peripheral decoding flow, and what GAL is involved in the decoding. The three frames group the peripherals into 8, 16 or 32-bit devices. The simple 3D-blocs represent an on-board device. The 3D-blocks with an arrow represent external devices (more generally: accessed through a connector).
GRANDS does the main decoding of peripherals and the 93xx-3 acquisition board.
PETITS does the sub-decoding for all 8-bit peripherals.
VIADUC handles the Motorola to Intel format decoding for the VGA controller.
CARDAN takes care of the PCMCIA interface timings.
PROFIL dispatches 8-bit data to the Centronics or the Floppy controller.
SAVEUR and SEVERE generate the serial clock and routes the data to the right serial device, including CLExxx, which is the option PAL.

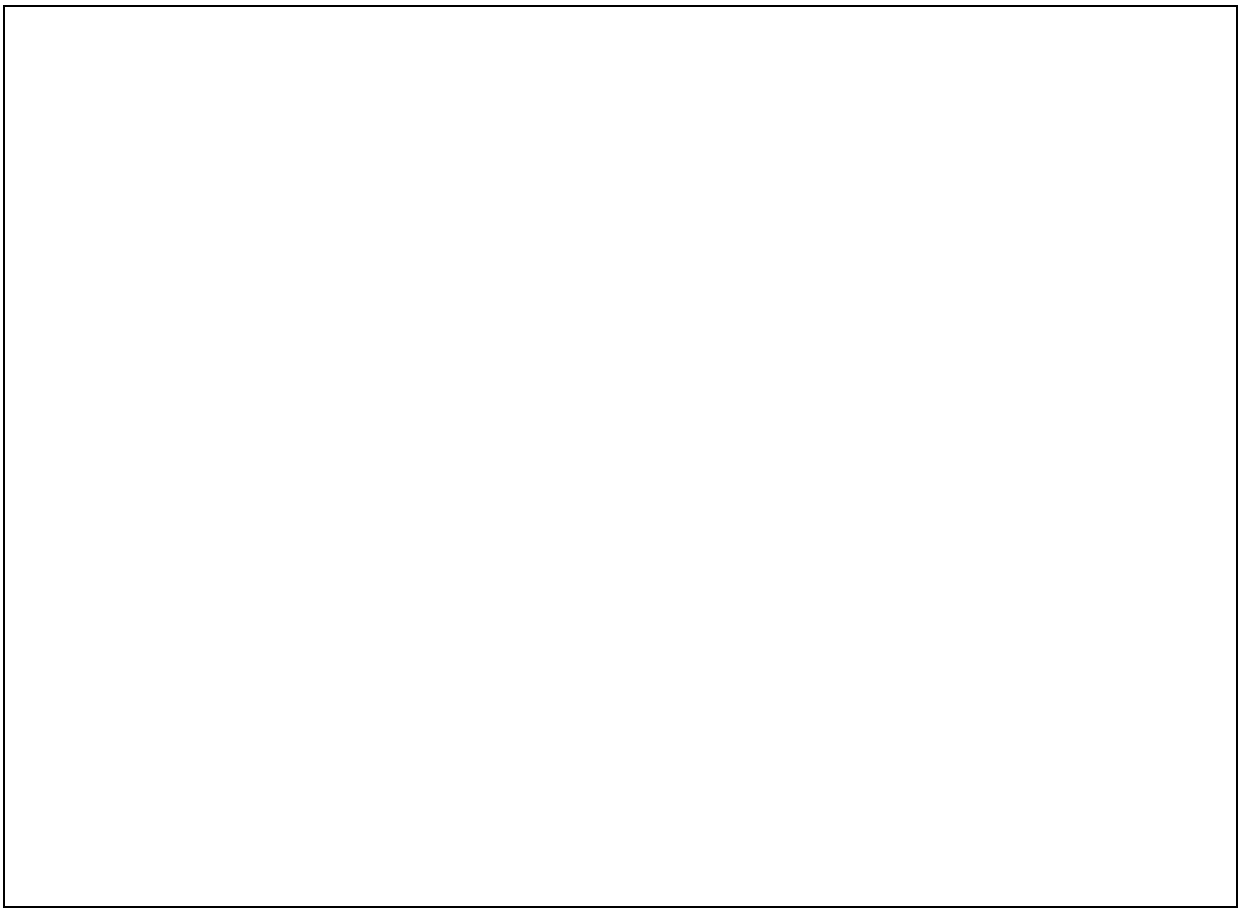

Fig 4-2: Peripheral Decoding and Data Bus Size

Not shown in Fig.4-2, are a few GALs for miscellaneous functions (like DRAM refreshing).
RASADE generates the RAS signals and the lower addresses for DRAM. It also supports the signals needed for interleaved burst mode.
OCCASE generates the CAS signals for DRAM.
RAMEUR is the main sequencer for the DRAM , and handles the access precharge and the refresh system.
BUDGET translates a 680x0 bus cycle into a PPC cycle, and handles fast cycles, like accesses to DRAM or VGA.
RETINE counts the wait states and generates a bus error if no response after too many (153) wait states. It also generates the system reset.
ASSISE decodes CPU space cycles and controls the bus sizer.

4.2 F9615-3 Main Board

4.2.1 Introduction

The board is divided into five sections :

- Microprocessor control based on the MTC428 EPLD pair.
- Front-end based on the Hybrid HFE444 & HSY430 switchyard board to combine the input channel.
- Trigger based on the Hybrids HTR420 discriminator & MST429A smart trigger
- Analog Converter based on the HAM435 Sample&Hold and A/D converter and MNX427 min/max to pre-compute the data.
- Digital Acquisition based on the HMM434 Acquisition memory and SIMM DRAM module for buffer memory.
- Time base based on the MCG426 clock generator & MTB411A controller

4.2.2 Front End

The front-end system provides the signal conditioning for the ADC system.
All channel are identical, thus only one channel will be described here.

The main functions of the Front end without the amplifier (HFE444) are:

- Four channels operation, calibration with Software control
- Input protection (clamp + thermal detection) and coupling (AC, DC, 1 MΩ, 50 Ω).
- Attenuator by 10 in the 50Ω path and attenuator by 20 in 1MΩ path.
- Offset control and CAL control.

The main functions of HFE444 are:

- Amplitude normalisation for the ADC system : at the BNC the dynamic range is 16 mV to 8V FS at 50Ω and to 16V FS (full scale) at 1 MOhm in a 1-2-5 step sequence and the ADC system input is 500 mV differential.
- Fine gain control to fill in the fixed vertical sensitivities.
- Bandwidth limit filter at 25 MHz and 200 MHz.

Power off State : 1 MΩ input

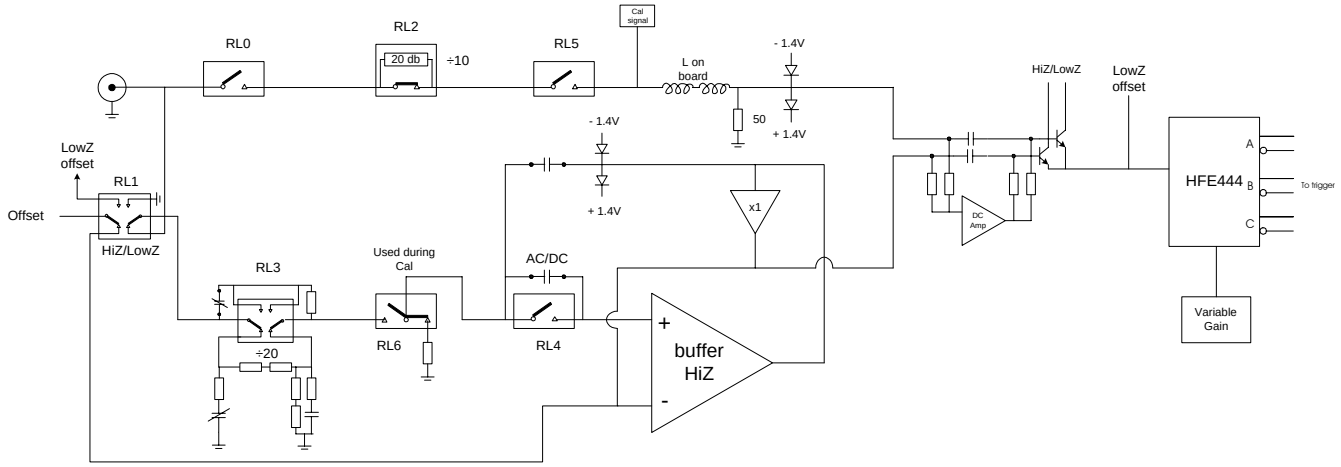

Fig 4-3: Front End Power off State

- Relay RL1 selects the input and offset voltage between the Hi-Z (1 MΩ) and the 50Ω path.
- The 50Ω path is then disconnected by RL0 and the signal will be in the 1 Mohm input.
- Relay RL2 selects the input between divide-by-10 or direct for the signal in the 50Ω path.
- Relay RL3 selects the input between direct or divide-by-20 for the signal in the HiZ path.
- Relay RL4 sets the AC/DC coupling in HiZ.
- Relay RL5 is only used during calibration.
- Relay RL6 clamps the HiZ amplifier when not selected..
- Bias_HiZ and Bias_LoZ is used to bias transistors Qx003 and Qx004 to select between the HiZ path or LowZ path as input to the HFE through the DC amplifier.
- There is no AC/DC coupling in the 50Ω path.

50Ω input : Direct Path

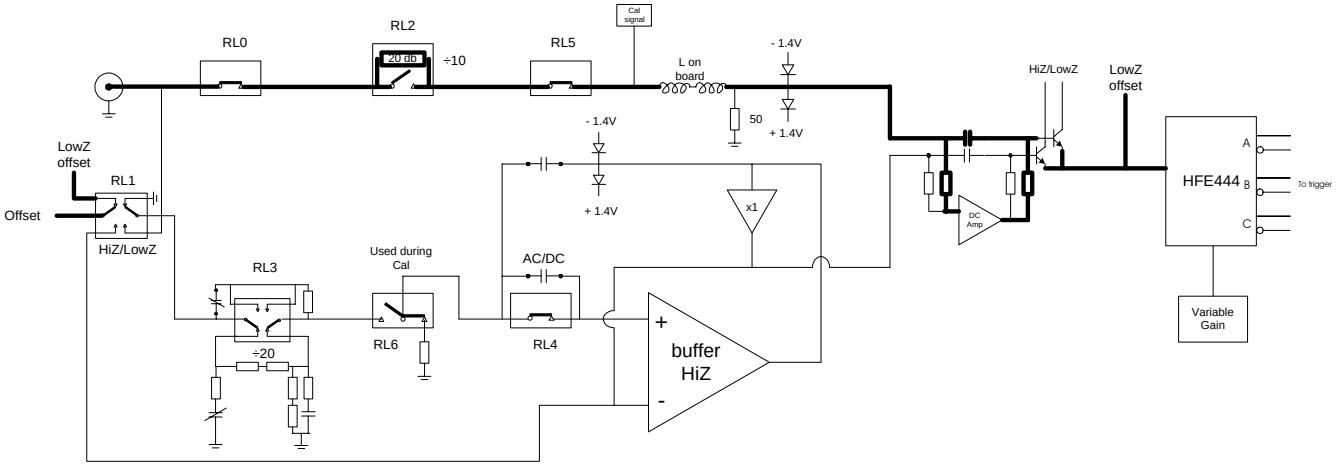

Fig 4-4: 50Ω input direct path

50Ω input : Divide-by-10 Path

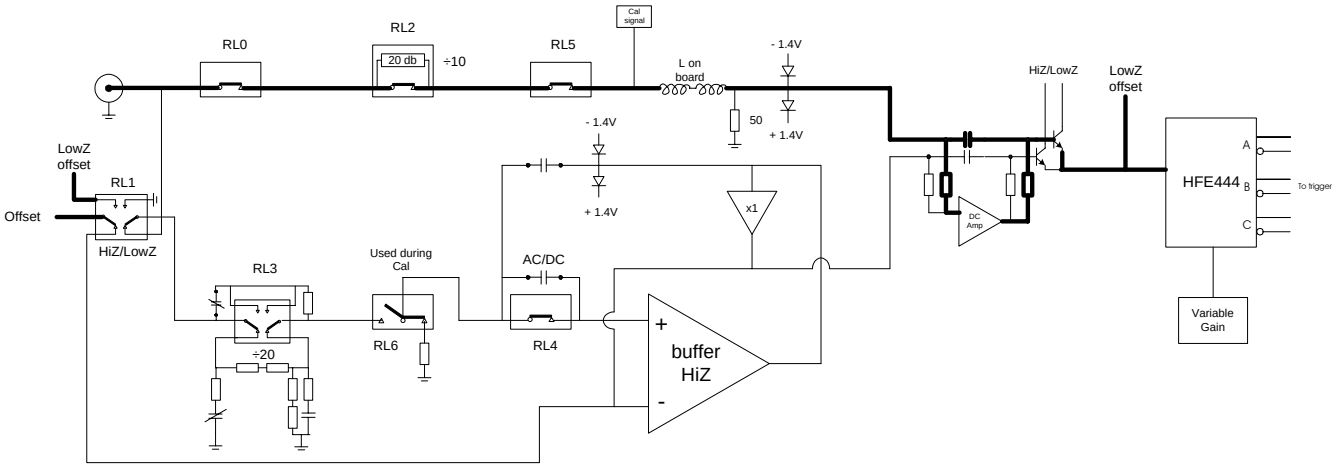

Fig 4-5: 50Ω divide by 10 path

1MΩ input : Direct Path

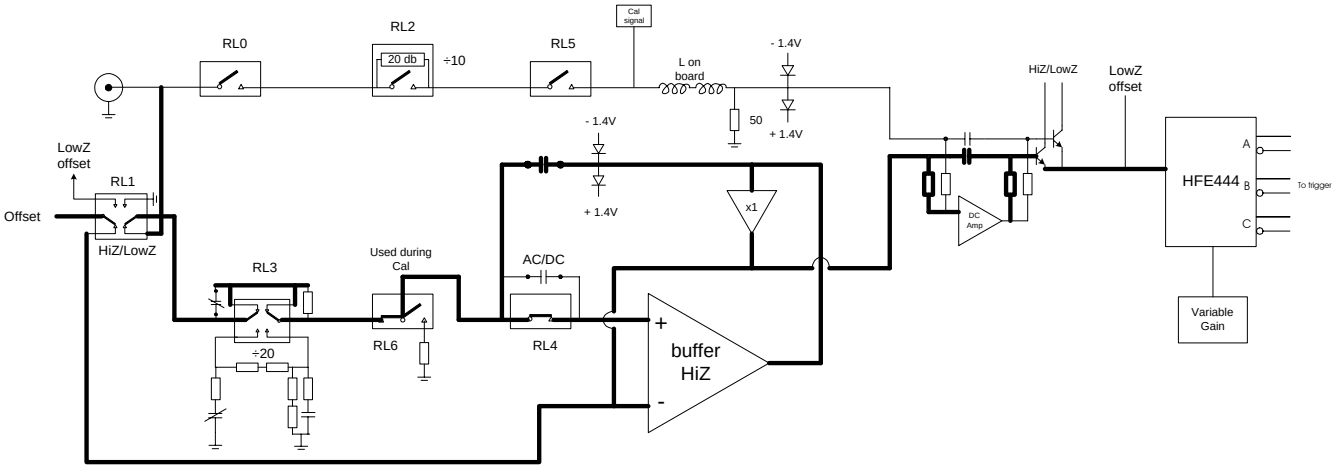

Fig 4-6: 1MΩ direct path

1MΩ divide by 10 AC coupled path

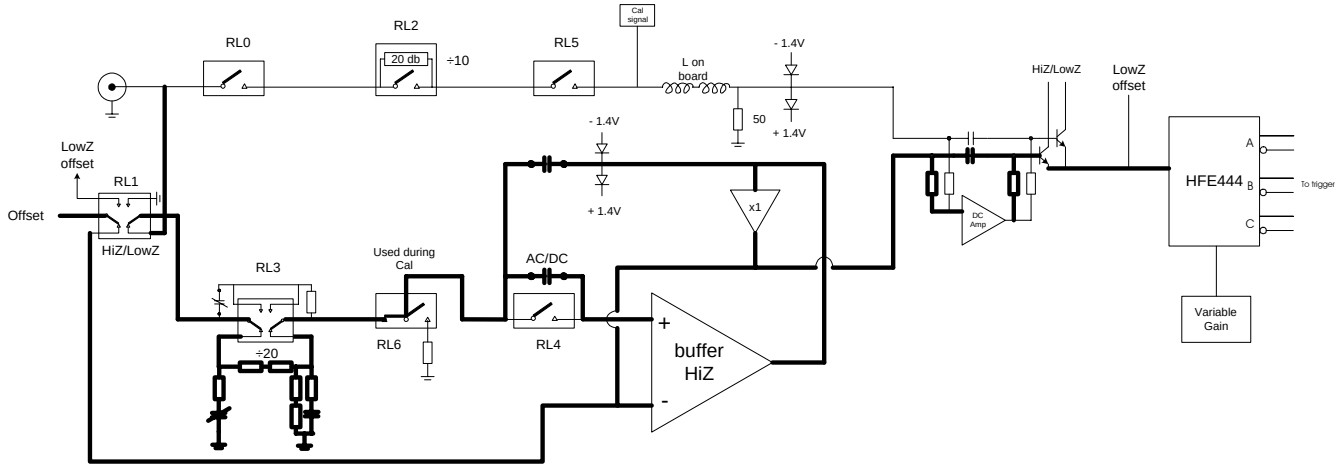

Fig 4-7: 1MΩ divide by 10 AC coupled path

Front End Analog controls

- One precision DAC with an associate circular memory (μP system) drives and refreshes a multiple sample-and-hold system. The DC calibration control is common to all four channels. Each channel has two analog controls.

4.2.3 F9615-3 Acquisition Block Diagram

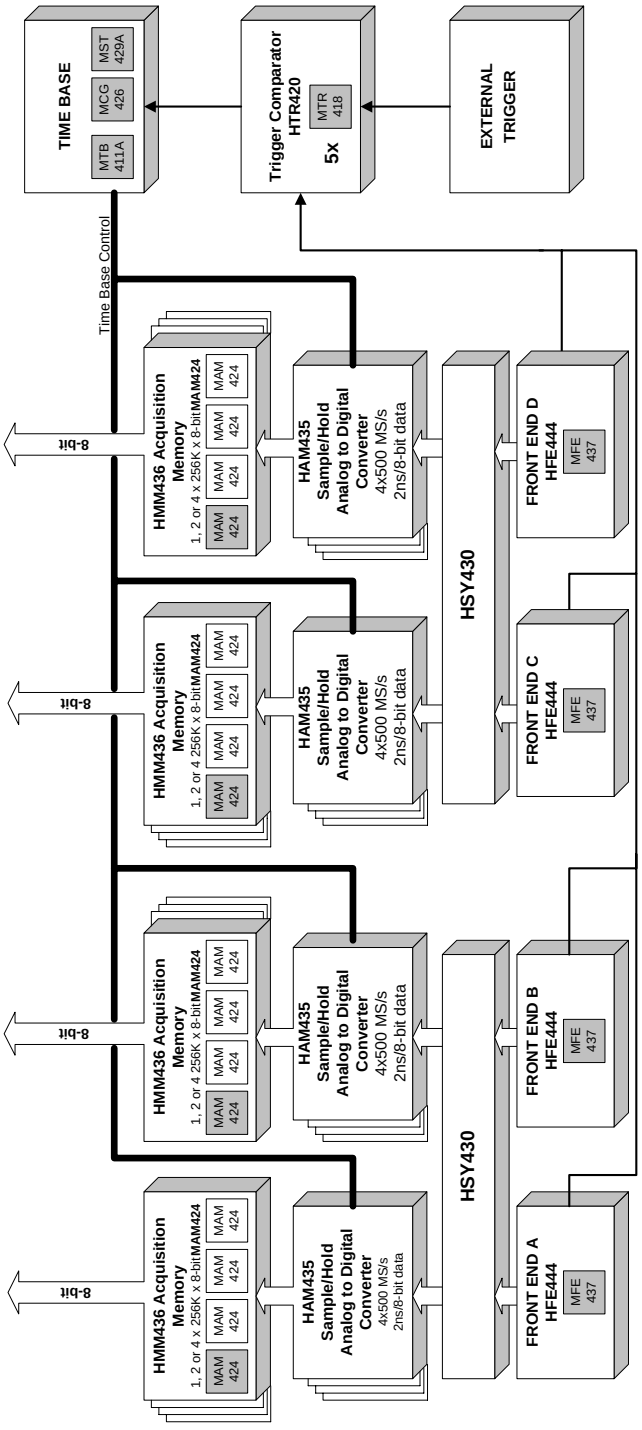

Fig 4.8: Front End, Trigger, Sample&Hold, Analog to Digital, Memory

4.2.4 One, Two and Four Channel mode

Four channel mode

- All BNC inputs are active

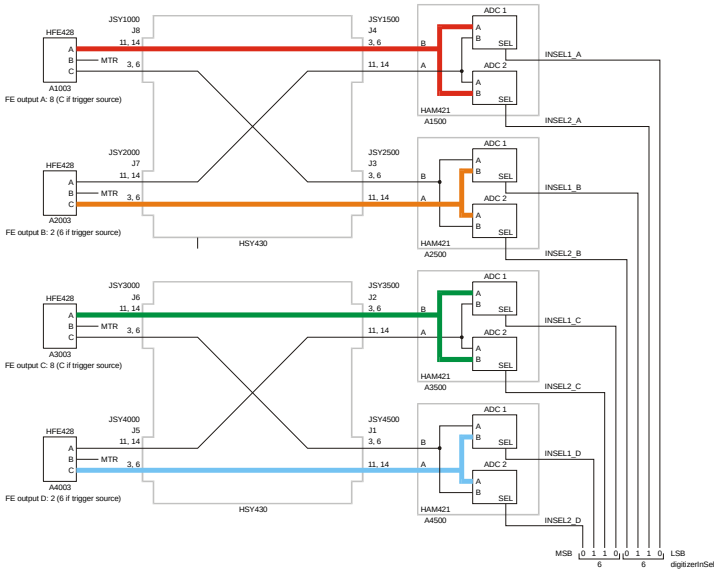

Figure 4-9 Four Channel Mode Signal Routing

One and Two channel mode

- Two channel mode, BNC inputs for channel 2 and 3 are active, ADC's for channel 1 & 2 are used for signal on channel 2 input, ADC's for channel 3& 4 are used for signal on channel 3 input.
- One channel mode, PP096 adapter must be connected between channel 2 and 3 BNC inputs, all 4 ADC's are used for signal input to PP096

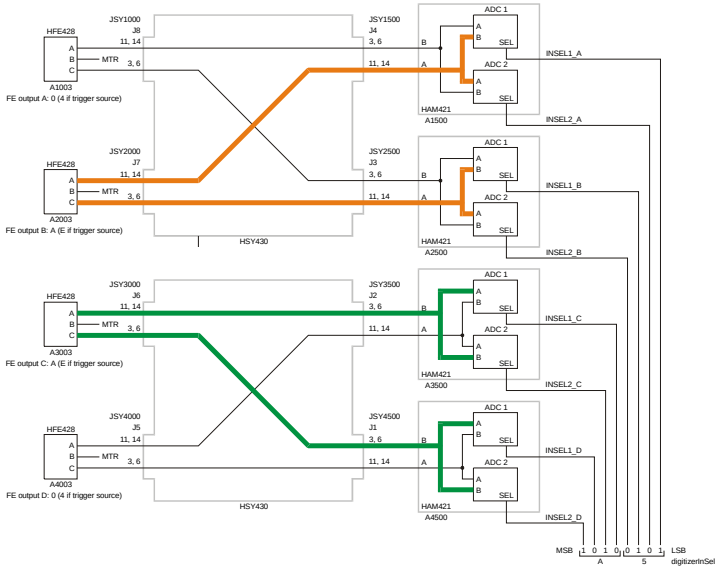

Figure 4-10 One and Two Channel Mode Signal Routing

4.2.5 F9615-3 Control & Transfer Block Diagram

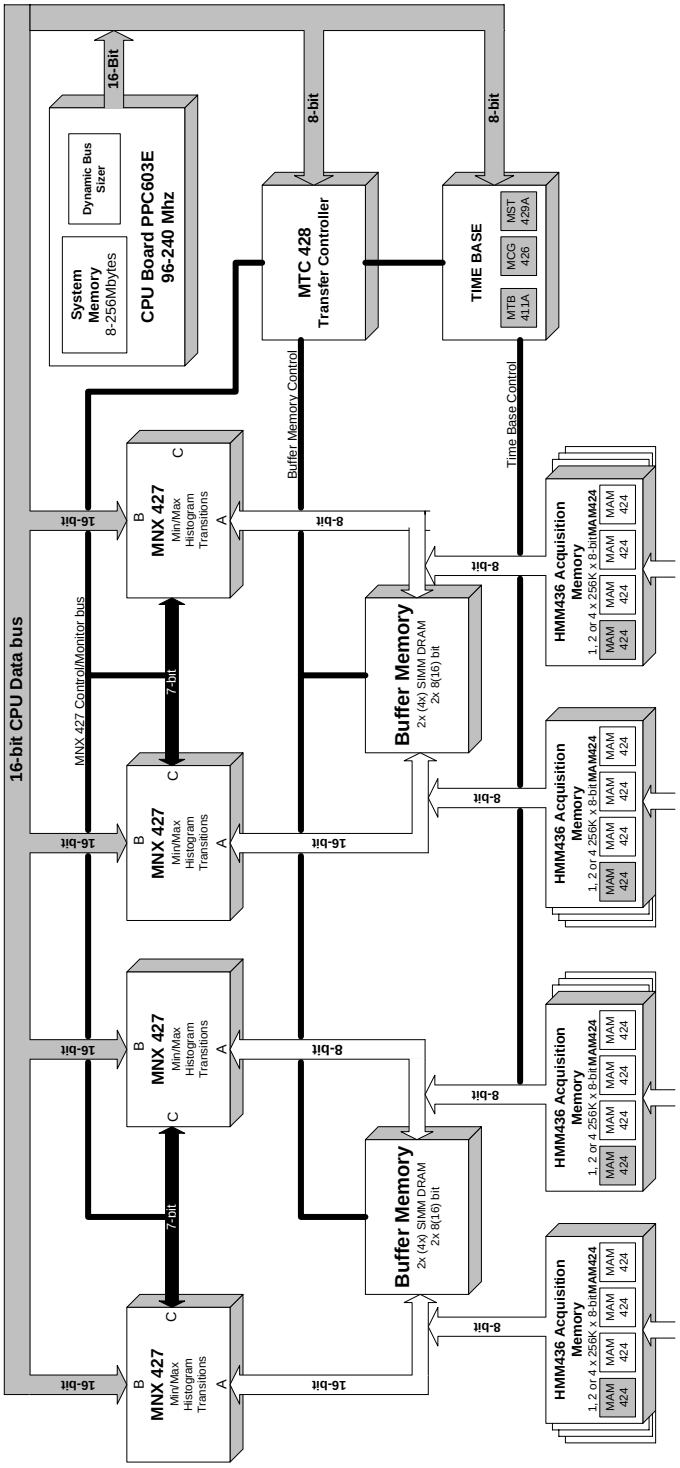

Fig 4.11: Processor Control, Min/Max, Buffer Memory, Transfer

4.2.5 Trigger

The different trigger couplings are :

- DC
- AC : cut off frequency is almost 10 Hz.
- LF REJ : single pole high pass filter with a cut off frequency at50 kHz.
- HF REJ : single pole low pass filter with a cut off frequency at 50 kHz.
- TBWL : single pole low pass filter at 25 MHz.

Analog Controls

A sample and hold fed by the precision DAC provides the threshold level.
The addresses are :

TV Trigger

Each channel has a pick-off after the HFE428 or after the high impedance buffer for external trigger. The TV trigger source is selected via bit TVS and drives a times 10 amplifier with complementary outputs. These outputs are selected (_TVINV) depending on the state of the selected HFE428 gain.
The TV trigger uses a commercial chip (LM1881) and provides two outputs, TV1 & TV2. This circuit is able to trigger on different TV line number standards.

4.2.6 Analog to Digital Converter

Introduction

The analog to digital converter system does the signal conversion to 8 bits, using the following circuits:

- **HAM435**: Hybrid Acquisition Module, Sample&Hold plus ADC

  MSH437: Monolithic Sample and Hold. performs the track&hold before the ADC.

  MAD422: Analog to Digital converter, maximum clock speed of 500 Ms/s

- **HMM436**: Hybrid Memory module, up to 4 Mbytes per Channel

  MAM 424: Monolithic Access Memory

- **MNX427**: Monolithic MIN-MAX

- **Buffer Memory** : 16Mbytes

- **HSY430**: Interleaving Channel

4.2.7 Time Base

Introduction

The time base includes three circuits:

- **MCG426**: generates sampling clocks: 12.5 MHz up to 2GHz
  generates clocks for the MTB411
  interleaves sampling clocks to increase sampling rate and memory depth.

- **MTB411A**: Time Base System
  TDC interpolator and Real Time computation
  Trigger circuitry
  Frequency divider

- **MST429A**: Single source trigger, Standard trigger, Hold off, Pulse width & interval
  Multiple source trigger, State qualified, Edge qualified

Block Diagram

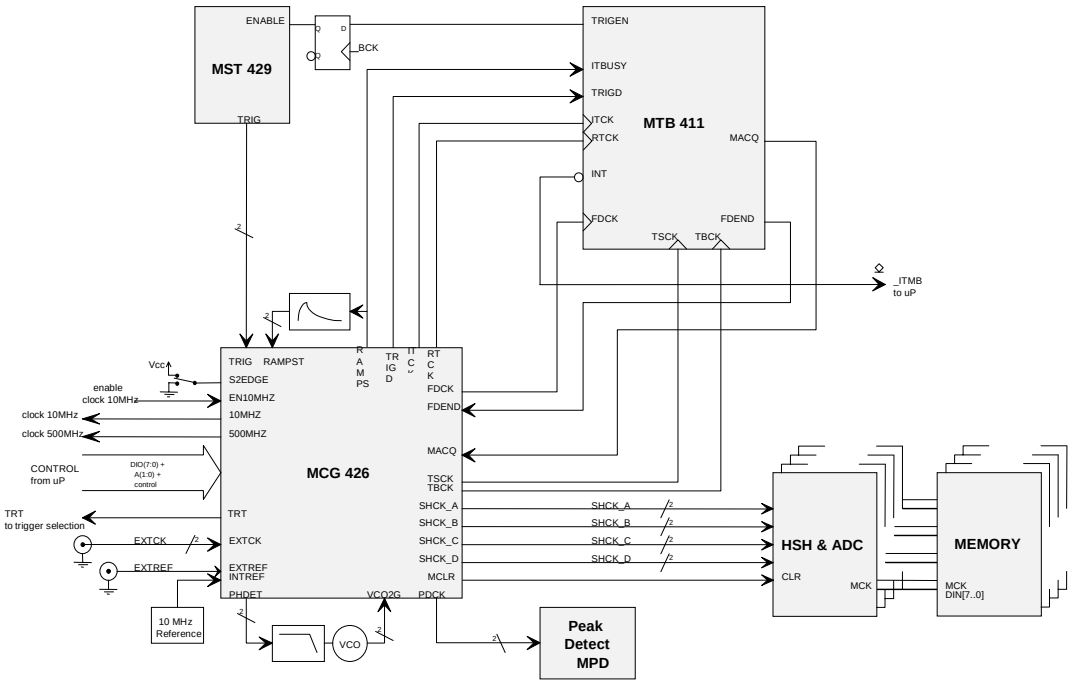

Fig 4.12: Time Base Block Diagram

4.3 F9301-4 GPIB and RS 232 Interface

4.3.1 Block Diagram

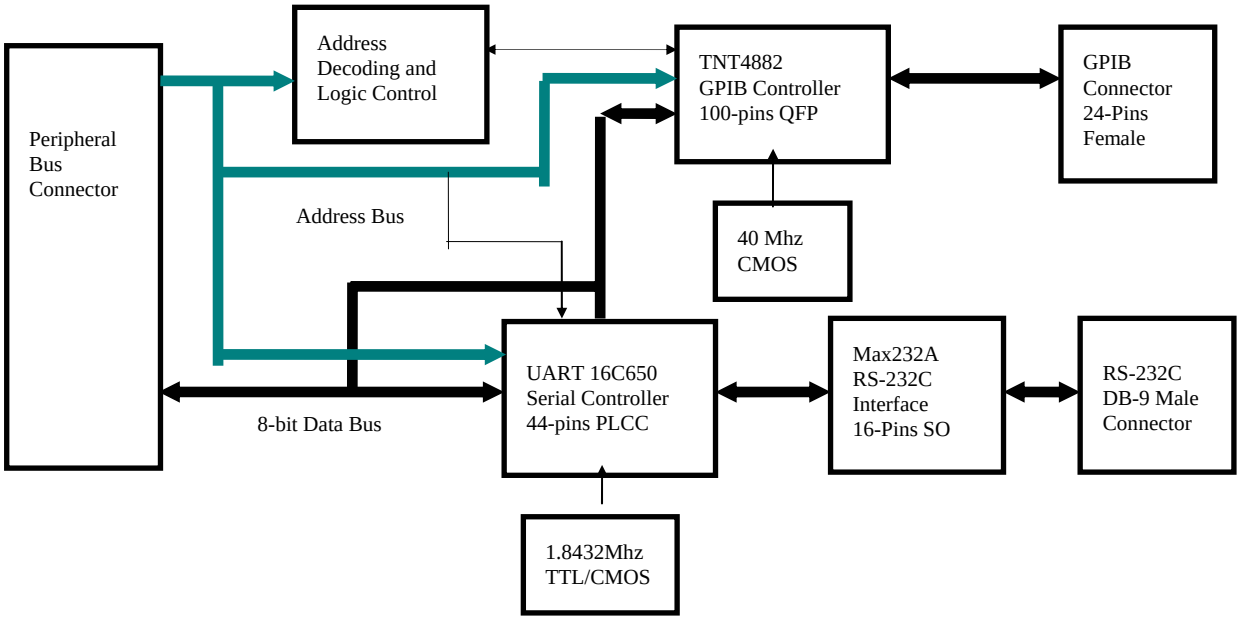

Fig 4.13: GPIB & RS232 Interface Block Diagram

This board is connected to the processor through a flat cable.
Data bus is 8 bits, address bus: 12 bits.
Address 0180 000 to 0180 00FF.

4.3.2 F9301-4 RS 232 Serial Interface

Based on the ST16650 from EXAR or Startech.

- Clock frequency 1.8432 MHz.
- RTC/CTS signals are connected
- DCD input is biased and the DTR output is not wired
- Asynchronous communication up to 1Mbits/sec
- 32 bytes receive and transmit FIFOs buffer
- Connector compatible with a DB9-P (9 pin male).

4.3.3 F9301-4 GPIB Interface

Based on the circuit TNT4882 from National Instruments.

- Clock frequency 40 MHz.
- Up to 1.5 Mbytes/sec using interlocked IEEE 488.1 handshake
- Two 8-bit 16-deep FIFOs buffer data between GPIB and CPU

The GPIB address is set by software and stored in non-volatile memory.

4.4 LCDFP9615 Front Panel

The front panel assy is connected to the processor board with a flat cable. Power supply and control signals are supplied from the processor. The front panel is divided into several sections:

- Display using 10.4inch TFT color LCD Module
- F9601-61 Floppy disk drive assy
- S9615-21 Buffer board which interfaces the digital signals from the processor to the TFT display unit
- S9615-52 board with Motorola 68HC05C4 processor, encoders, and serial data interface.
- F9615-5 matrix keypad with push buttons.

4.5 F9300-7 Printer Controller Option

- Based on the Internal graphic printer LPT5446, and LPT5000 series control chip set from Seiko instrument Inc (Technical reference 39019-2234-01)
- PT501P01 CPU
- PT500GA1 Gate array
- Address 0130 0100
- Interrupt level 2

4.6 PS9611 Power Supply

The PS9611 is a nine output 300 W AC-DC switching mode power supply.

4.6.1 Specifications

AC Input Voltage

85-132VAC and 170-264VAC, auto-ranging universal input, provides automatic sensing of 115 or 230VAC input voltage. Power factor correction for compliance with EN61000-3-2: 1995 standard (harmonic current emissions) under all conditions of input voltage, input frequency, loads and temperature ranges.
AC power enters the DSO chassis thru an IEC320 input receptacle, fuses and an EMI line filter. The filter high frequency noise generated by the DSO from getting out on to the AC line.

Input Frequency: AC input Frequency range of 47 Hz to 63 Hz.

Inrush Current: less than 30 A over full line voltage ranges and input frequency

DC Output Specifications

Output	Adjustment Range	Nominal Load	Maximum Load
+5 (1)	+4.8 to +5.4V	15A	20A
+3 (1)	+2.9 to +3.5V	10A	20A
-2 (1)	-1.9 to –2.6V	5A	15A
-5 (1)	-4.8 to -5.4V	15A	20A
+6 (1)	+5.6 to +6.2V	2.5A	4A
-6 (1)	-5.6 to -6.2V	2.5A	4A
+15	+14.8 to +15.4V	2.5A	4A
-15	-14.8 to -15.4V	2A	3A / 8A
-12	-11.5 to -14.0V	0.5A	1A

Note:(1) with remote sense.

Output power: 300W

Ripple and Noise: less than 25 mV

Hold up Time: 25 mV at full load

Transient response: recovery time <1.2 msec to within 50 mV of its final value

Protections: over current, over voltage, over temperature

Cooling: PS9611 is cooled by a forced airflow provided by a fan that is integrated inside the unit.

Environmental: Operating temperature range 0 °C to + 55 °C
Storage temperature range - 55 °C to + 85 °C
Operating humidity from 5% to 95% RH.
Operating Altitude (max) 5000m or 15000 feet

Safety Standards: CE, UL, CSA, TUV
EN61010-1:1993 (IEC1010-1:1995), UL3111-1,
CSA-C22.2 No.61010-1.
Protection class I, pollution degree 2, installation category II.

EMI: EN50081-1:1992, EN55022:1987 Class B, EN61000-3-2&3:1995 Class D

Immunity: EN50082-1:1994, EN61000-4-2,4,5,8&11:1995,
IEC1000-4-2,3,4,5,6,8&11

4.6.2 Power Supply Block Diagram